HEWLETT-PACKARD COMPANY
Intellectual Property Administration
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Fort Collins, Colorado 80527-2400

ORIGINAL

PATENT APPLICATION

ATTORNEY DOCKET NO. 200302320-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Timothe LITT

Confirmation No.: 1520

Application No.: 10/034,717

Examiner: T. M. Bonura

Filing Date: 12/28/2001

Group Art Unit: 2114

Title: METHOD AND APPARATUS FOR EFFICIENTLY IMPLEMENTING TRACE AND/OR LOGIC ANALYSIS MECHANISMS ON A PROCESSOR CHIP

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on 09/01/2005.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
( )	two months	$450.00
( )	three months	$1020.00
( )	four months	$1590.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of $500.00. At any time during the pendancy of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Number of pages: 28

Typed Name: Jessica R. Beedle

Signature: Jessica R. Beedle

Respectfully submitted,

Timothe LITT

By _____

Alan D. Christenson

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Date: 11/01/2005

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COPY

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Typed Name: Jessica R. Beedle

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Timothe LITT

By /Alan Christenson/

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Timothe LITT	§	Confirmation No.:	1520
Serial No.:	10/034,717	§	Group Art Unit:	2114
Filed:	12/28/2001	§	Examiner:	Timothy M. Bonura
For:	Method And Apparatus For Efficiently Implementing Trace And/Or Logic Analysis Mechanisms On A Processor Chip	§	Docket No.:	200302320-1

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Date: November 1, 2005

Sir:

Appellant hereby submits this Appeal Brief in connection with the above-identified application. A Notice of Appeal was filed via facsimile on September 1, 2005.

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I. REAL PARTY IN INTEREST

The real party in interest is the Hewlett-Packard Development Company (HPDC), a Texas Limited Partnership, having its principal place of business in Houston, Texas. HPDC is a wholly owned affiliate of Hewlett-Packard Company (HPC). HPC merged with Compaq Computer Corporation (CCC) which owned Compaq Information Technologies Group, L.P. (CITG). CCC merged with Digital Equipment Corporation DEC with CCC being the surviving entity. The Employee Agreement with the inventor and DEC and the Articles of Merger from DEC to CCC, the Assignment from CCC to CITG and the Change of Name document were recorded on February 23, 2004, at Reel/Frame 014993/0547.

II. RELATED APPEALS AND INTERFERENCES

Appellant is unaware of any related appeals or interferences.

III. STATUS OF THE CLAIMS

Originally filed claims:	1-29.
Claim cancellations:	None.
Added claims:	None.
Presently pending claims:	1-29.
Presently appealed claims:	1-4, 6, 12-16, 21, 25, 27.
Objected to claims:	The Examiner indicated that dependent claims 5, 8-11, 17-20, 22-24, 26, and 28-29 contain allowable subject matter.

IV. STATUS OF THE AMENDMENTS

Amendments to claims 2-11 and 20 were submitted after filing the Notice of Appeal to correct a formality. In an Advisory Action dated September 16, 2005, the Examiner indicated that for purposes of appeal, the amendments will be entered. Accordingly, Appellant assumes the amendments have been entered. The Claims Appendix includes claim 2-11 and 20 as amended.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The following provides a concise explanation of the subject matter defined in each of the claims involved in the appeal, referring to the specification by page and line number and to the drawings by reference characters, as required by 37 C.F.R. § 41.37(c)(1)(v). Each element of the claims is identified by a corresponding reference to the specification and drawings where applicable (*i.e.*, the claims are annotated using parenthesis). Note that the citation to passages in the specification and drawings for each claim element does not imply that the limitations from the specification and drawings should be read into the corresponding claim element.

1. (Original) An integrated circuit fabricated on a chip (see Fig. 1 and ¶ [0024]), comprising:

an on-chip logic analyzer (125) (see Fig. 1 and ¶ [0027]);

a cache memory (150) that includes a plurality of cache sets (see Fig. 1 and ¶ [0024]-[0025]);

at least one on-chip logic device (110) that stores data to said plurality of cache sets during normal operation (see Fig. 1 and ¶ [0025]); and

a logic gate (195) that receives an enable signal when the on-chip logic analyzer (125) is enabled, and which disables at least one of said plurality of said cache sets for storing data from said on-chip logic analyzer (125) (see Fig. 1 and ¶ [0030]).

2. (Previously presented) The integrated circuit of claim 1, wherein the integrated circuit comprises a processor (100), and the on-chip logic device (110) includes a CPU core (110) (see Fig. 1 and ¶ [0024]-[0025]).

3. (Previously presented) The integrated circuit of claim 2, wherein the enable signal ("Qen") is generated by the on-chip logic analyzer (125) (see Fig. 1 and ¶ [0030]).

4. (Previously presented) The integrated circuit of claim 3, wherein the logic (195) comprises a multiplexer (335) that connects the on-chip logic analyzer (125) to the disabled cache set (350) when the on-chip logic analyzer (125) asserts the enable signal ("Qen") (see Figs. 1, 3A, 3B and ¶ [0038]-[0039]).

6. (Previously presented) The integrated circuit of claim 1, wherein the on-chip logic analyzer (125) receives information regarding internal state data of the processor (100) and selects some of the received information for storage in the disabled cache set (350) (see Figs. 1, 2, 3A, 3B and ¶ [0028]-[0030] and [0039]).

12. (Original) A processor (100), comprising:
a CPU core (110);
a cache memory (150) coupled to said CPU core (110), said cache memory (150) including a plurality of cache sets that during normal operation store data written by the CPU core (110); and
at least one logic analyzer (125) that receives information relating to the internal state of the processor (100), said logic analyzer (125) being coupled to at least one of said plurality of cache sets, and wherein said logic analyzer (125) is capable of gaining ownership of said at least one cache set to store selected portions of said received information when said on-chip logic analyzer (125) is enabled (see Fig. 1 and ¶ [0024], [0025] and [0030]).

13. (Original) The processor (100) of claim 12, further comprising a multiplexer (335) that couples to said CPU core (110) via a first bus ("CPU") and which couples to said logic analyzer (125) via a second bus ("Q"), and wherein said multiplexer (335) selects either said first bus ("CPU") or said second bus ("Q") to connect to said at least one cache set (350) (see Figs. 1, 3A, 3B and ¶ [0039]).

14. (Original) The processor (100) of claim 13, wherein said multiplexer (335) receives an enable signal ("Qen") indicating whether to connect said first bus ("CPU") or said second bus ("Q") to said at least one cache set (350) (see Figs. 1, 3A, 3B and ¶ [0039]).

15. (Original) The processor (100) of claim 13, wherein the logic analyzer (125) is located on-chip (see Fig. 1 and ¶ [0027]).

16. (Original) The processor (100) of claim 13, wherein said multiplexer (335) couples to test logic (175) via third bus ("Test"), and wherein said multiplexer (335) selects one of said first bus ("CPU"), said second bus ("Q"), or said third bus ("Test") to connect to said at least one cache set (350) (see Figs. 1, 3A, 3B and ¶ [0039]).

21. (Original) A processor (100) fabricated on a chip, comprising:
a cache memory (150) divided into a plurality of cache sets;
test logic (175) coupled to said cache memory (150), which tests the cache sets during system initialization and determines which cache sets are operative;
a cache controller (135) that controls the storage and retrieval of data from said cache memory (150), with said cache controller (135) only storing data to cache sets that are determined to be operative by the test logic (175);
a CPU core (110) coupled to said cache memory (150), said CPU core (110) storing data to all operative cache sets during normal operation;
an on-chip logic analyzer (125) capable of receiving data reflecting the internal state of the processor (100), said on-chip logic analyzer (125) coupled to at least one cache set, which is disabled from use by the CPU core (110) when the on-chip logic analyzer (125) is enabled (see Fig. 1 and ¶ [0024], [0025] and [0030]).

25. (Original) A method of maintaining state data of a processor (100) in a cache memory set (350), comprising the acts of:

enabling an on-chip logic analyzer (125) to receive and select data for storage;

disabling a cache set (350) from use by any device other than the on-chip analyzer (125);

storing said selected data in the disabled cache set (125) (see Figs. 1, 3A, 3B and ¶ [0030] and [0039]).

27. (Original) The method of claim 25, wherein the act of disabling the cache set (350) includes transmitting an enable signal ("Qen") to a multiplexer (335) that selects the on-chip logic analyzer (125) as the sole source of data to be written to the cache set (350) (see Figs. 3A, 3B and ¶ [0039]).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-4 and 6 are anticipated by U.S. Pat. No. 6,618,775 ("Davis").

Whether claims 12-16 are anticipated by Davis.

Whether claim 21 is anticipated by Davis.

Wherein claims 25 and 27 are anticipated by Davis.

VII. ARGUMENT

The claims do not stand or fall together. Instead, Appellant presents separate arguments for various independent and dependent claims. Each of these arguments is separately argued below and presented with separate headings and sub-heading as required by 37 C.F.R. § 41.37(c)(1)(vii).

A. Overview of Davis

Davis is directed to a digital signal processor (DSP) that incorporates a bus monitor. The bus monitor includes bus watching circuitry, circular buffers, and an external interface. Davis' Figure 6 shows a bus monitor that monitors DSP busses in accordance with Davis.

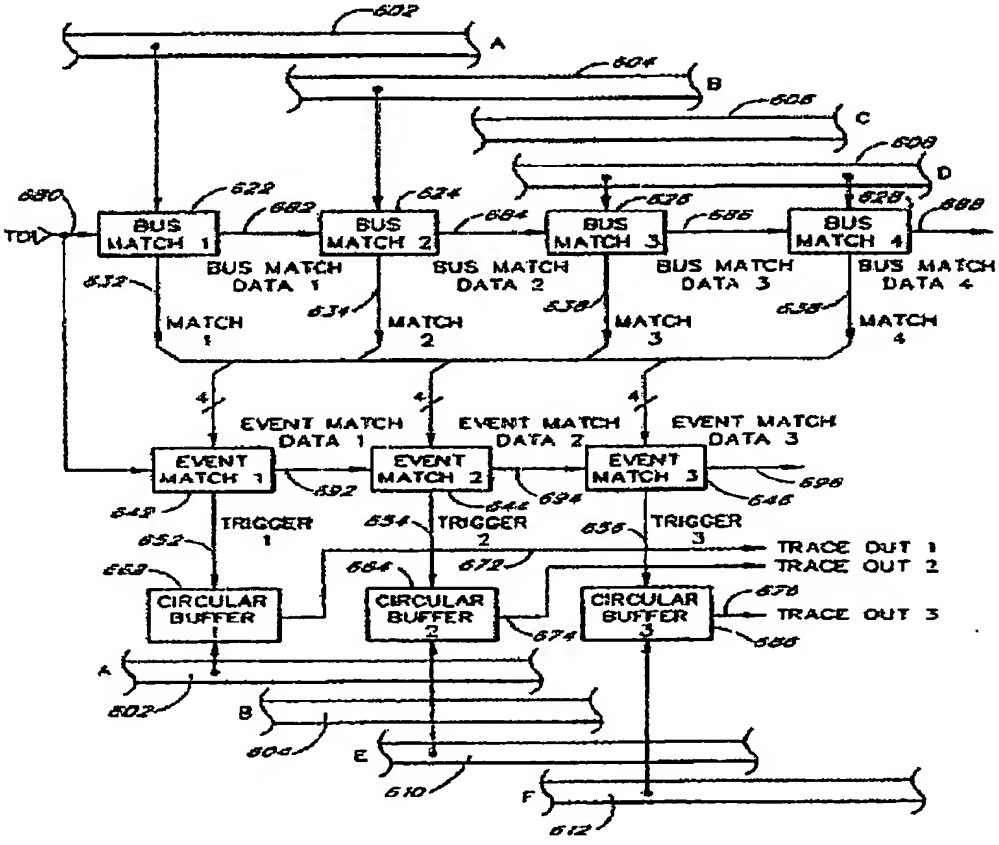


FIG. 6

In describing Figure 6, Davis states

> [t]he bus watching circuitry includes multiple bus matching functions and event matching functions to generate multiple circular buffer triggers. Each bus match circuit monitors a bus to determine the occurrence of a particular bus event, generating a "match" signal in response.

Col. 4, lines 21-25

> Each event match circuit responds to a particular combination of these match signals to generate a trigger signal to a particular circular buffer.

Col. 4, lines 37-39

> These circular buffers each are connected to a processor bus and continually store valid data to a bus until a trigger signal is detected. Each circular buffer responds to its trigger signal input to stop the storage of data from its particular processor bus.

Col. 4, lines 50-54

> After detecting a trigger signal, trace data obtained from a processor bus is retained in a circular buffer until it is uploaded to an external device or until the buffer is reset.

Col. 4, lines 60-62

Based on the foregoing, Davis simply teaches that circular buffers can be used to continuously store processor bus data (by overwriting the oldest data in a "circular" fashion) until a trigger event occurs. When the circular buffer stops storing data, the data retained in the circular buffer may be provided to an external interface for analysis and display. Importantly, Davis does not teach or suggest using an existing cache memory or cache sets with the bus monitor. Instead, Davis teaches using dedicated memory (circular buffers) separate from "data caches" mentioned by Davis (see col. 2, lines 1-6).

B. Claims 1-4 and 6, with claim 1 representing this group

Davis does not anticipate claim 1 as suggested by the Examiner. "A claim is anticipated only if each and every element as set forth in the claim is found, each expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v Union Oil Co. of California*, 814 F.2d 628, 631.

Appellant's claim 1 requires "an on-chip logic analyzer" and "a cache memory that includes a plurality of cache sets." Claim 1 further requires "at least

one on-chip logic device that stores data to said plurality of cache sets during normal operation" and "a logic gate that receives an enable signal when the on-chip logic analyzer is enabled, and which disables at least one of said plurality of said cache sets for storing data from said on-chip logic analyzer."

In rejecting claim 1, the Examiner equates the circular buffers taught in Davis with Appellant's claimed "cache memory" or "cache sets." However, the terms "cache memory" and "circular buffers" are not inherently equivalent. Appellant submits that the terms "circular buffer" and "cache" are different terms commonly used by those of ordinary skill in the computing industry. For example, Computer Dictionary Online defines a "cache" as "[a] small fast memory holding recently accessed data, designed to speed up subsequent access to the same data." See http://www.computer-dictionary-online.org/index.asp?q=cache. Also, Computer Dictionary Online defines a "circular buffer" as "[a]n area of memory used to store a continuous stream of data by starting again at the beginning of the buffer after reaching the end." See http://www.computer-dictionary-online.org/index.asp?q=circular+buffer. This definition of "circular buffer" coincides with the description of circular buffers in Davis, which states "[the] circular buffers each are connected to a processor bus and continually store valid data to a bus until a trigger signal is detected" (col. 4, lines 50-54).

Even if the circular buffers were to be considered equivalent to a "cache memory" or "cache sets" as suggested by the Examiner, Davis fails to teach Appellant's claimed "at least one on-chip logic device that stores data to said plurality of cache sets during normal operation" and "a logic gate that receives an enable signal when the on-chip logic analyzer is enabled, and which disables at least one of said plurality of said cache sets for storing data from said on-chip logic analyzer." In simple terms, each circular buffer of Davis is only intended to store data from a single bus line (see Figure 6 and col. 4, lines 52-54). In contrast, at least one of Appellant's claimed "cache sets" stores data from the "on-chip logic device" and from the "on-chip logic analyzer." Based on the foregoing, Appellant respectfully submits that Davis does not anticipate any of

claims 1-4 and 6 under 35 U.S.C. § 102 and the rejection of this grouping should be reversed.

C. Claims 12-16, with claim 12 representing this group

Claim 12 requires "a CPU core" and "a cache memory coupled to said CPU core, said cache memory including a plurality of cache sets that during normal operation store data written by the CPU core." Claim 12 further requires "at least one logic analyzer that receives information relating to the internal state of the processor, said logic analyzer being coupled to at least one of said plurality of cache sets, and wherein said logic analyzer is capable of gaining ownership of said at least one cache set to store selected portions of said received information when said on-chip logic analyzer is enabled."

As previously described, the Examiner equates the circular buffers of Davis with Appellant's claimed "cache memory" and "cache sets" even though circular buffers are commonly understood to be different than Appellant's claimed "cache memory" and "cache sets." Even if the circular buffers of Davis were to be considered equivalent to a "cache memory" or "cache sets" as suggested by the Examiner, Davis still fails to teach Appellant's claimed "a cache memory coupled to said CPU core, said cache memory including a plurality of cache sets that during normal operation store data written by the CPU core" and "at least one logic analyzer that receives information relating to the internal state of the processor, said logic analyzer being coupled to at least one of said plurality of cache sets, and wherein said logic analyzer is capable of gaining ownership of said at least one cache set to store selected portions of said received information when said on-chip logic analyzer is enabled." Again, each circular buffer of Davis is only intended to store data from a single bus line (see Figure 6 and col. 4, lines 52-54). In contrast, claim 12 requires that at least one of the "cache sets" stores "data written by a CPU core" and stores "selected portions of said received information when [an] on-chip logic analyzer is enabled." Based on the foregoing, Appellant respectfully submits that Davis does not anticipate any of claims 12-16 under 35 U.S.C. §102 and the rejection of this grouping should be reversed.

D. Claim 21

Claim 21 requires "a cache memory divided into a plurality of cache sets" and "test logic coupled to said cache memory, which tests the cache sets during system initialization and determines which cache sets are operative." Claim 21 further requires "a cache controller that controls the storage and retrieval of data from said cache memory, with said cache controller only storing data to cache sets that are determined to be operative by the test logic" and "a CPU core coupled to said cache memory, said CPU core storing data to all operative cache sets during normal operation." Claim 21 further requires "an on-chip logic analyzer capable of receiving data reflecting the internal state of the processor, said on-chip logic analyzer coupled to at least one cache set, which is disabled from use by the CPU core when the on-chip logic analyzer is enabled."

As previously described, the Examiner equates the circular buffers of Davis with Appellant's claimed "cache memory" and "cache sets" even though circular buffers are commonly understood to be different than Appellant's claimed "cache memory" and "cache sets." Even if the circular buffers of Davis were to be considered equivalent to a "cache memory" or "cache sets" as suggested by the Examiner, Davis still fails to teach Appellant's claimed "test logic coupled to said cache memory, which tests the cache sets during system initialization and determines which cache sets are operative." There is simply no test circuit in Davis that tests the circular buffers "during system initialization" as required in claim 21.

Further, Davis does not teach "a CPU core coupled to said cache memory, said CPU core storing data to all operative cache sets during normal operation" and "an on-chip logic analyzer capable of receiving data reflecting the internal state of the processor, said on-chip logic analyzer coupled to at least one cache set, which is disabled from use by the CPU core when the on-chip logic analyzer is enabled" as required in claim 21. Based on the foregoing, Appellant respectfully submits that Davis does not anticipate claim 21 under 35 U.S.C. §102 and the rejection of this grouping should be reversed.

E. Claims 25 and 27, with claim 25 representing this group

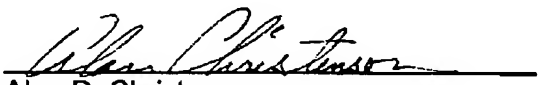
Claim 25 requires "enabling an on-chip analyzer to receive and select data for storage" and "disabling a cache set from use by any device other than the on-chip analyzer." Claim 25 further requires "storing said selected data in the disabled cache set."

As previously described, the Examiner equates a circular buffer of Davis with Appellant's claimed "cache set" even though a circular buffer is commonly understood to be different than Appellant's claimed "cache set." Even if the circular buffer of Davis were to be considered equivalent to a "cache set" as suggested by the Examiner, Davis still fails to teach Appellant's claimed "disabling a cache set from use by any device other than the on-chip analyzer" and "storing said selected data in the disabled cache set." As previously described, each circular buffer is only intended to store data from a single bus line (see Figure 6 and col. 4, lines 52-54) and thus cannot be "disabled...from use by any device other than the on-chip analyzer" as required of Appellant's claimed "cache set." Based on the foregoing, Appellant respectfully submits that Davis does not anticipate any of claims 25 and 27 under 35 U.S.C. § 102 and the rejection of this grouping should be reversed.

VIII. CONCLUSION

For the reasons stated above, Appellant respectfully submits that the Examiner erred in rejecting all pending claims. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,



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IX. CLAIMS APPENDIX

1. (Original) An integrated circuit fabricated on a chip, comprising:
an on-chip logic analyzer;
a cache memory that includes a plurality of cache sets;
at least one on-chip logic device that stores data to said plurality of cache sets during normal operation; and
a logic gate that receives an enable signal when the on-chip logic analyzer is enabled, and which disables at least one of said plurality of said cache sets for storing data from said on-chip logic analyzer.

2. (Previously presented) The integrated circuit of claim 1, wherein the integrated circuit comprises a processor, and the on-chip logic device includes a CPU core.

3. (Previously presented) The integrated circuit of claim 2, wherein the enable signal is generated by the on-chip logic analyzer.

4. (Previously presented) The integrated circuit of claim 3, wherein the logic comprises a multiplexer that connects the on-chip logic analyzer to the disabled cache set when the on-chip logic analyzer asserts the enable signal.

5. (Previously presented) The integrated circuit of claim 4, wherein the multiplexer forms part of a cache controller.

6. (Previously presented) The integrated circuit of claim 1, wherein the on-chip logic analyzer receives information regarding internal state data of the processor and selects some of the received information for storage in the disabled cache set.

7. (Previously presented) The integrated circuit of claim 6, further comprising a second on-chip logic analyzer that receives information regarding instructions

executing in the processor, and wherein the second on-chip logic analyzer selects at least some of said received information for storage in the disabled cache set.

8. (Previously presented) The integrated circuit of claim 7, wherein the disabled cache set is sub-divided into multiple portions, and said on-chip logic analyzer and said second on-chip logic analyzer are each assigned a portion of said disabled cache set.

9. (Previously presented) The integrated circuit of claim 1, further comprising a cache controller that couples to said cache memory and which controls accesses to said cache memory, and wherein data stored by the on-chip logic analyzer is assigned an address range, and said cache controller forces a hit on said disabled cache set when a read request is made to the address range assigned to the on-chip logic analyzer.

10. (Previously presented) The integrated circuit of claim 1, wherein data stored by the on-chip logic analyzer is assigned an address range, and said disabled cache set makes available at least a portion of the data stored therein when a read request is made to the address range assigned to the on-chip logic analyzer.

11. (Previously presented) The integrated circuit of claim 10, wherein the on-chip logic analyzer includes an addressable read register that receives data stored in the disabled cache set in response to a read request to an address range assigned to the on-chip logic analyzer.

12. (Original) A processor, comprising:
a CPU core;
a cache memory coupled to said CPU core, said cache memory including a plurality of cache sets that during normal operation store data written by the CPU core; and

at least one logic analyzer that receives information relating to the internal state of the processor, said logic analyzer being coupled to at least one of said plurality of cache sets, and wherein said logic analyzer is capable of gaining ownership of said at least one cache set to store selected portions of said received information when said on-chip logic analyzer is enabled.

13. (Original) The processor of claim 12, further comprising a multiplexer that couples to said CPU core via a first bus and which couples to said logic analyzer via a second bus, and wherein said multiplexer selects either said first bus or said second bus to connect to said at least one cache set.

14. (Original) The processor of claim 13, wherein said multiplexer receives an enable signal indicating whether to connect said first bus or said second bus to said at least one cache set.

15. (Original) The processor of claim 13, wherein the logic analyzer is located on-chip.

16. (Original) The processor of claim 13, wherein said multiplexer couples to test logic via third bus, and wherein said multiplexer selects one of said first bus, said second bus, or said third bus to connect to said at least one cache set.

17. (Original) The processor of claim 16, wherein said multiplexer receives a first enable signal from said logic analyzer and a second enable signal from said test logic, and wherein said multiplexer selects which of said first, second or third bus to connect to said at least one cache set based on the status of said first and second enable signals.

18. (Original) The processor of claim 17, wherein said multiplexer awards priority to said logic analyzer if said logic analyzer requests access to said at least one cache set.

19. (Original) The processor of claim 12, wherein data stored by the logic analyzer is assigned an address range, and said at least one cache set makes available at least a portion of the data stored therein when a read request is made to the address range assigned to the logic analyzer.

20. (Previously presented) The processor of claim 19, wherein the logic analyzer includes an addressable read register that receives data stored in the at least one cache set in response to a read request to an address range assigned to the on-chip logic analyzer.

21. (Original) A processor fabricated on a chip, comprising:
a cache memory divided into a plurality of cache sets;
test logic coupled to said cache memory, which tests the cache sets during system initialization and determines which cache sets are operative;
a cache controller that controls the storage and retrieval of data from said cache memory, with said cache controller only storing data to cache sets that are determined to be operative by the test logic;
a CPU core coupled to said cache memory, said CPU core storing data to all operative cache sets during normal operation;
an on-chip logic analyzer capable of receiving data reflecting the internal state of the processor, said on-chip logic analyzer coupled to at least one cache set, which is disabled from use by the CPU core when the on-chip logic analyzer is enabled.

22. (Original) The processor of claim 21, wherein data stored by the on-chip logic analyzer is assigned an address range, and said cache controller forces a

hit on said disabled cache set when a read request is issued to the address range assigned to the on-chip logic analyzer.

23. (Original) The processor of claim 22, wherein the on-chip logic analyzer includes an addressable read register that receives data stored in the disabled cache set in response to the read request to an address range assigned to the on-chip logic analyzer.

24. (Original) The processor of claim 21, wherein the on-chip logic analyzer is capable of issuing a read request to the cache controller for data stored in the disabled cache set, which includes a signal indicating that the cache controller should force a hit on the disabled cache set.

25. (Original) A method of maintaining state data of a processor in a cache memory set, comprising the acts of:

enabling an on-chip logic analyzer to receive and select data for storage;

disabling a cache set from use by any device other than the on-chip analyzer;

storing said selected data in the disabled cache set.

26. (Original) The method of claim 25, further comprising the acts of:

reading said selected data from said disabled cache set; and

storing said data read from the disabled cache set to an addressable register.

27. (Original) The method of claim 25, wherein the act of disabling the cache set includes transmitting an enable signal to a multiplexer that selects the on-chip logic analyzer as the sole source of data to be written to the cache set.

28. (Original) The method of claim 26, wherein the act of reading selected data includes:

issuing a read request to an I/O address reserved for on-chip logic analyzer data;

recognizing the read request as targeting on-chip logic analyzer data;

routing the read request to the cache memory; and

forcing a hit on the disabled cache set.

29. (Original) The processor of claim 17, wherein said test logic will preserve the contents of at least one said cache set during a reset operation if said first enable signal is asserted.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

None.